Proceedings of ICRC 2001: 1 © Copernicus Gesellschaft 2001

ICRC 2001

A systematic study of the ARGO Experiment Front-End Electronics

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Abstract. The Front-End Electronics performing the ARGO RPCs readout is a full custom 8 channels GaAs circuit. About 19000 FE boards are foreseen for the experiment. We describe here the selection criteria applied by means of a systematic test devoted to check the dynamic functionality of each single channel. The statistical results from more than 20000 analysed channels are presented.

1 Introduction

The Front-End Electronics performing the ARGO RPCs readout [1][2][3] is a full custom 8 channels GaAs circuit, which integrates in a single die both the analog and digital signal processing. The die is bonded on the Front-End Board which is mounted on the pick-up strips panel and therefore completly closed inside the detector Farady cage. This peculiarity avoids the use of interconnession cables that would degrade the analog signals transmitted to the FE Electronics. It requires however to certificate the complete functionality of the FE board before detector assembling.

2 The Electronics and the Experimental Set-Up

The Electronics global function is to amplify, discriminate and convert to ECL standard the detector signals. It is based on a three stage voltage amplifier and on a comparator with variable threshold [4],[5],[6],[7]. When dedicated to detectors working in streamer mode the chip amplification (~ 340) is too large. A resistor partition (P~ 0.15), displaced at each channel input on FE board, is applied on the input signal to attenuate the overall amplification. The block diagram with a simplified scheme of the full signal processing is sketched in figure 1.

A DC electric test is performed, before and after the bonding of the die on the board, by the involved companies. The test is devoted to check the continuity of electrical lines, the right power consumption and the correct voltage levels, in inputs and outputs, with respect to the applied voltage threshold on comparator.

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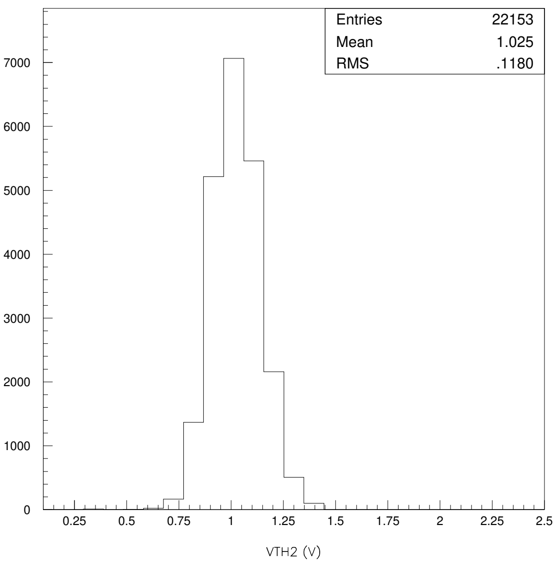

Fig. 3. The Voltage Threshold distribution, at fixed input signal, for 22153 tested channels.

An AC test is performed by the ARGO group of ”Tor Vergata” University of Rome. The test checks the dynamic functionality of each single channel and selects FE boards to be assembled on the detector. It measures and registers all relevant electronics parameters to build up a complete database for the experiment.

The experimental set-up is composed by a pulse generator and a VXIbus armed with a controller VXI-MXI board interfaced with a VXI-PCI board inside an appropriate Personal Computer. A software program (BridgeView) running on the PC controls each step and performs the complete AC test automatically. An RF switching module injects the in-

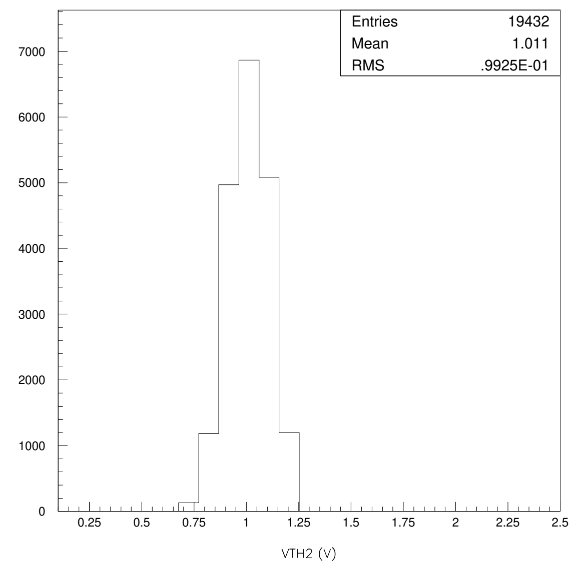

Fig. 4. The Voltage Threshold distribution for all selected channels.

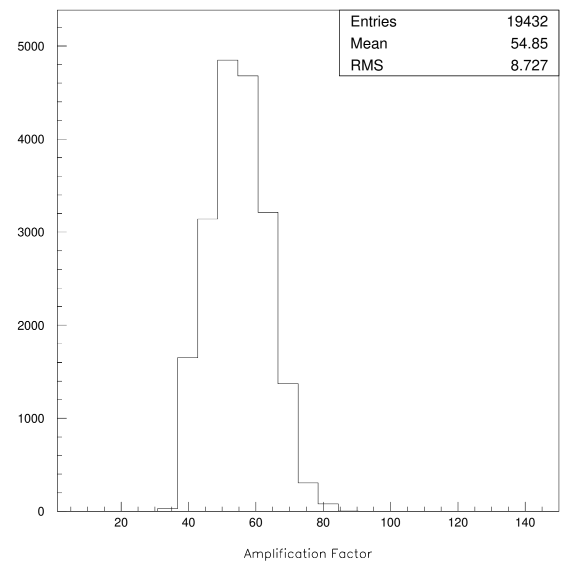

Fig. 5. The resulting distribution of the overall amplification factor of the FE electronics.

put signal in the eight FE board input channels by means of a dedicated probe system, developed to minimize signal degradation and any noise source. A waveform analyzer module, characterized by 5 GSample/s digitizing rate and 1 GHz of analog bandwidth, continuously monitors the output signal. A D/A module produces the low voltage supplies, an A/D converter module reads out DC voltage levels. A simplified scheme of the experimental set-up is shown in figure 2.

The full system guarantees for fast signal transmission and provides high-speed signal acquisition.

3 The AC Test

Each FE board is identified by a bar code, printed on a proper label, and tested according the following procedure.

The low voltage applied power supply (VEE), the fixed voltage threshold on comparator (VTH1), the power consumption at each amplification and digital stage (Ia,Ib,Ic,Id) are measured, together with the environment temperature (T).

A fixed input signal of 10 mV amplitude and 30 ns time duration (2.3 ns rise time) from generator is injected into each channel. Such signal simulates the expected average signal from pick-up strips of read-out. The variable voltage threshold (VTH2) is increased until the output signal, continuously monitored by the waveform analyzer, is recognized as an ECL standard signal easily detectable by a line receiver. The corresponding VTH2 value is recorded.

A large sample of 2853 FE boards, corrisponding to 22824 channels, was tested. The VTH2 distribution for all 22153 channels with good functionality is shown in figure 3.

Channels with defected functionality cause the exclusion of the FE board. The failure rate of channels is 2.9 per cent leading to an 85.1 per cent yield of the FE Boards.

A window of acceptable VTH2 levels is fixed around the mean value. The greater accepted VTH2 value, corresponding in the test logic to the lowest amplification power, must be compatible with the maximum expected efficiency of the detector. Channels with good functionality but low amplification can be corrected by modifying the resistor partition at channel input.

The good or corrected channels with VTH2 values between 0.7 and 1.2 V are selected to be mounted on the detector. The distribution shown in figure 4 is the characteristic 'response dispersion' for these 19432 selected channels.

In figure 5 the corresponding full amplification factor of the FE electronics is shown, its mean value is 55$\pm$9. This includes the attenuation factor of 0.15 due to the input voltage divider.

The VTH2 distribution versus the eight channels of the chip, shown in figure 6, guarantees a good uniformity with respect to the threshold necessary for the full detector efficiency.

The average power consumption per channel is (22$\pm$2) mW, its distribution is shown in figure 7.

All the control parameters of the Electronics do not have any significant temperature dependence. In figure 8 are shown the scatter plots for the VTH1 voltage levels, for the VTH2 distribution and for the power consumption of the digital stage Id.

Acknowledgements. The authors are indebted to Professor R.Santonico for encouragement and useful suggestions, to E.Pastori for the technical contribution and the Italian MURST (Ministero dell'Universitá e della Ricerca Scientifica e Tecnologica) for the financial support.

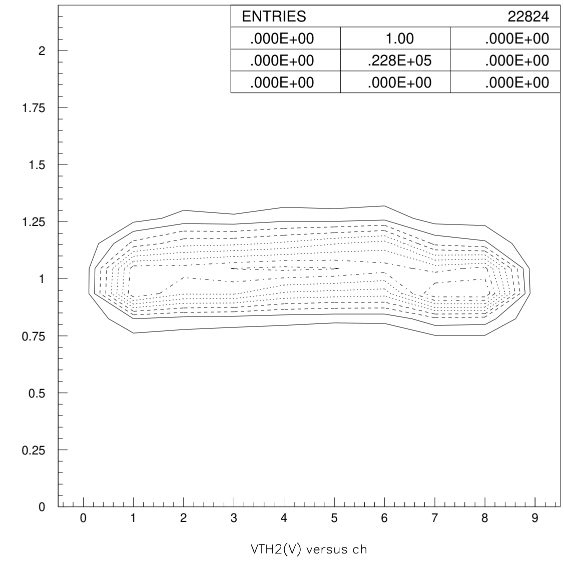

Fig. 6. The Vth2 thresold versus the chip channels.

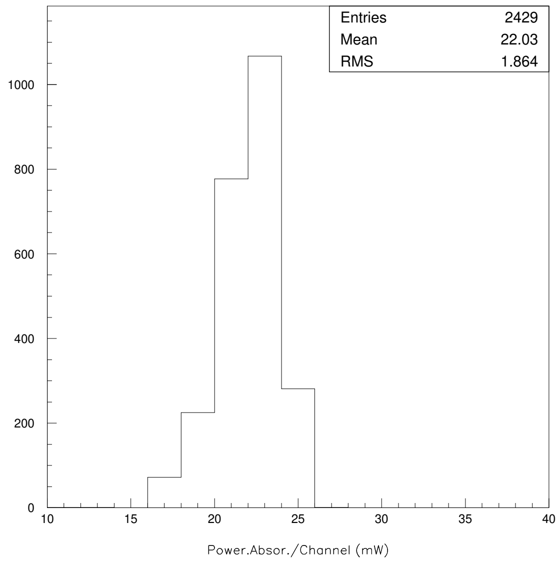

Fig. 7. The Power Consumption Distribution per channel.

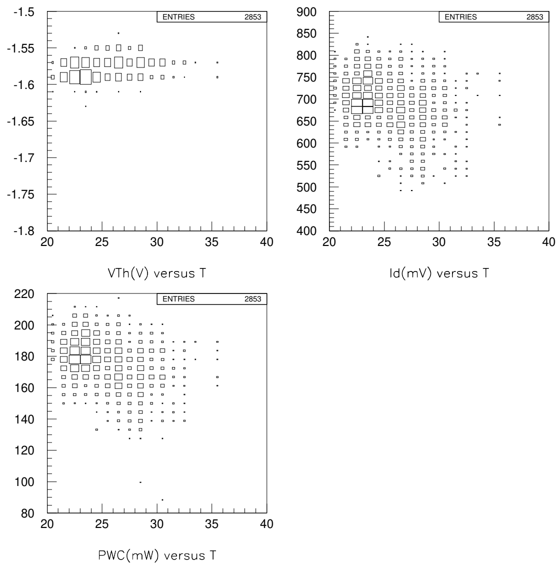

Fig. 8. The VTH1 threshold level, the VTH2 threshold distribution and the power consumption at digital stage Id versus environment temperature.

References

1. C.Bacci et al, "The use of RPC in the ARGO-YBJ project", Nuclear Physics B (Proc. Supp.) 78 (1999) 38-43.
2. C.Bacci et al., "High altitude test of RPC's for the ARGO-YBJ experiment", NIM Nuclear Instruments and Methods in Physics Research A443 (2000) 342-350.
3. Abbrescia M. et al., "Astroparticle Physics with ARGO, Proposal (1996).
4. R.Cardarelli,S.Ciorciolini,V.Chiostri,G.Orengo, "An 8-channels GaAs IC front-end discriminator for RPC particle detectors", GAAS 98 Conference, Amsterdam 1998.
5. G.Orengo,R.Cardarelli,S.Ciorciolini,E.Johansen, "Multichannels GaAs MMIC front-end gas chamber particle detectors", GAAS 97-European Gallium Arsenide and related III-V compounds Application Symposium, Bologna, Italy 1997.
6. R.Cardarelli,S.Ciorciolini,V.Chiostri,G.Orengo, "8-channels GaAs IC front-end discriminator for RPC particle detectors", IV International Workshop on Resistive Plate Chamber and Related Detectors, Napoli, Italy 1997.
7. G.Aielli et al., "RPC front-end electrnics for the ATLAS Level 1 Trigger detector", NIM, Nuclear and Instruments Methods in Physics Research A409 (1998).

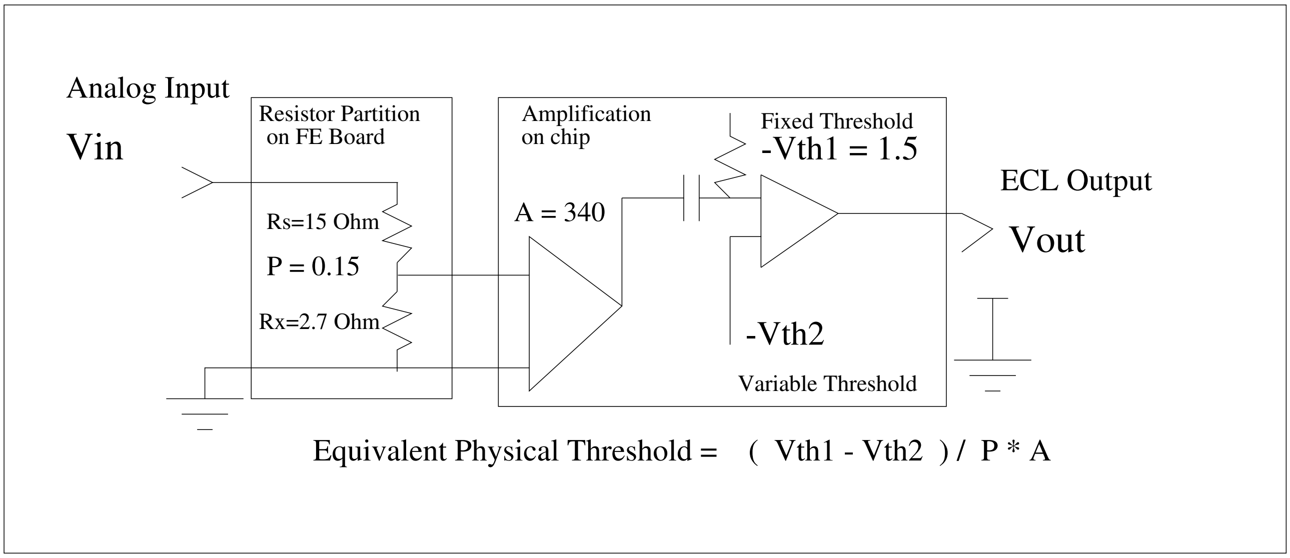

Fig. 1. The simplified scheme of signal processing.

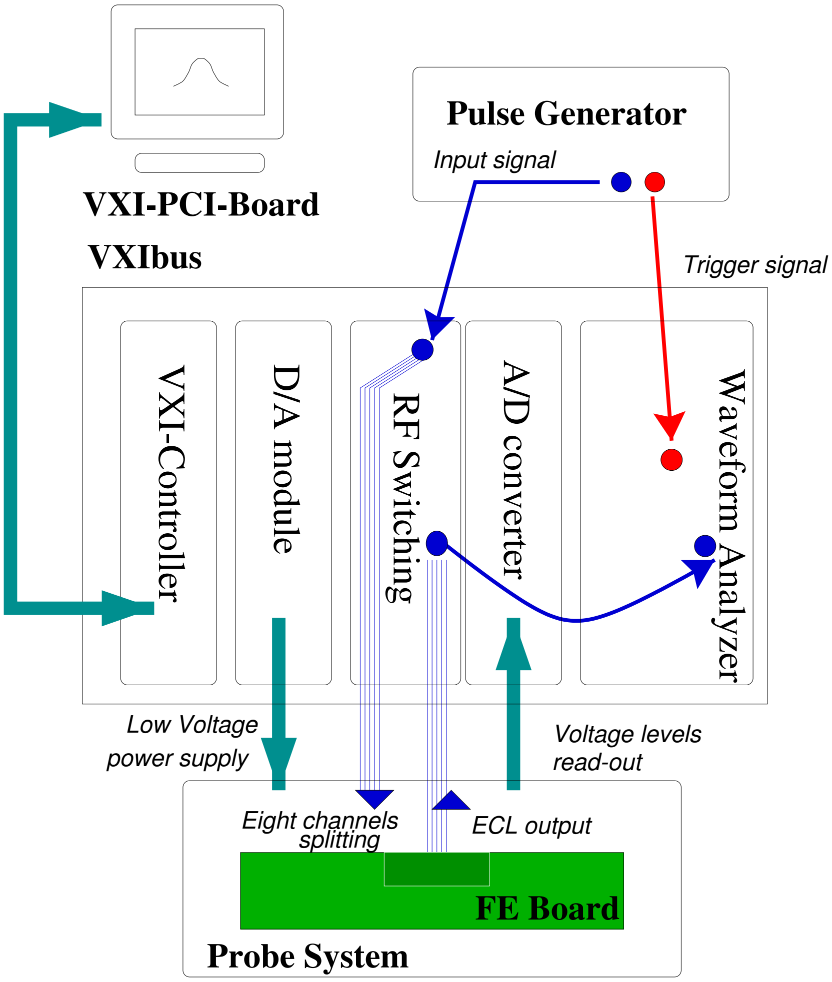

Fig. 2. The experimental set-up for test is composed by: a pulse generator (HFS9003 STIMULUS SYSTEM Tektronix), an appropriate Personal Computer, a VXIbus (IntelliFrame Mainframe VX1410A Tektronix) armed with a controller board (VXI-MXI-2 National Instruments), a 12 channels D/A module (VX4730 Tektronix), an RF switching module (VX4320 Tektronix), a 32 channels A/D converter module (VX4287 Tektronix) and a waveform analyzer module (TVS625A Tektronix). The dedicated probe system was specifically developed by the working group.